# AXI PROTOCOL

Using separate address and data channels for read and write transfers helps to maximize the bandwidth of the interface. There is no timing relationship between the groups of read and write channels. This means that a read sequence can happen at the same time as a write sequence.

Each of these five channels contains several signals, and all these signals in each channel have the prefix as follows:

• AW for signals on the Write Address channel

• AR for signals on the Read Address channel

• W for signals on the Write Data channel

• R for signals on the Read Data channel.

• B for signals on the Write Response channel (B stands for buffered, because the response from the subordinate happens after all writes have completed.)

Each channel is unidirectional, so a separate Write Response channel is needed to pass responses back to the manager. However, there is no need for a Read Response channel, because a read response is passed as part of the Read Data channel.

Read and write handshakes must adhere to the following rules:

• A source cannot wait for READY to be asserted before asserting VALID.

• A destination can wait for VALID to be asserted before asserting READY.

These rules mean that READY can be asserted before or after VALID, or even at the same time